

ABSTRACT OF THE DISCLOSURE

Methods and apparatuses for a data processing system are described herein. In one aspect of the invention, an exemplary apparatus includes a chip interconnect, a memory controller for controlling the host memory comprising DRAM memory, the memory controller coupled to the chip interconnect, a scalar processing unit coupled the chip interconnect wherein the scalar processing unit is capable of executing instructions to perform scalar data processing, a vector processing unit coupled the chip interconnect wherein the vector processing unit is capable of executing instructions to perform vector data processing, and an input/output (I/O) interface coupled to the chip interconnect wherein the I/O interface receives/transmits data from/to the scalar and/or vector processing units.

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